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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,235	03/30/2001	Hong Wang	10559-401001 / P10338	6323

20985 7590 11/08/2004

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,235	WANG ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, and 5-39 have been examined.

Papers Received

2. Receipt is acknowledged of Amendment papers submitted, where the papers have been placed of record in the file.

3. The objections to the abstract, title, and drawings as well as the 35 USC 112 rejections have all been successfully overcome by the amendment and are herein withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5-10, 15-18, and 20-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Nair et al (Exploiting Instruction level Parallelism in Processors by Caching Scheduled Groups).

6. In regard to claim 1, Nair discloses an apparatus comprising:

a. a cache of trace information associated with a plurality of traces, each of the plurality of traces including information indicative interdependent instructions, which interdependent instructions include at least an associated instruction and a criterion instruction that is part of a program sequence and which is data dependent on said associated instruction; [Figure 1 shows the use of a DIF

cache and the paragraph above the figure shows that this cache stores reformatted or translated sequences of previously executed instructions and is thus a trace cache based on the definition known in the art. Further proof is as follows: Figure 2 illustrates a trace of instructions. Figure 7 illustrates the traces of figure 2 after translation or reformatting and thus as stored in the cache or trace cache. The specification defines a criterion instruction in the replacement paragraph (for the paragraph beginning on page 4, line 18) on page 3 of the amendment to be a branch or a load that can incur long latency when executed. The cached instructions of figure 7 include a criterion instruction as the second "lwz" (load) instruction of slot 3. This criterion instruction is data dependent on an associated instruction in the lwz instruction of slot 2, which is an associated instruction because of the data dependency. This criterion instruction has a source (R6.2, a register) that is the same as the destination of the associated instruction (R6.2) and thus is data dependent. Traces or groups 0-3 are a plurality of traces and each contain a criterion instruction according to the definition. As shown in figure 7, these instructions are a part of an instruction sequence including other interdependent instructions. Therefore, the traces of Nair shown in figure 7 include the interdependent instructions, which is information indicative or identifying the interdependent instructions.]

b. And one or more processors that speculatively execute interdependent instructions associated with a first trace of the plurality of traces as a result of detecting a first triggering condition corresponding to the first trace. [As shown in

figure 7, the 2nd and 3rd instructions of slot 1 are executed on the condition that the branch (ble) is not taken. The branch and the instructions thereafter are speculatively executed (with a prediction that it is not taken), as described on page 20, column 1, until the branch is verified.]

7. In regard to claim 2, Nair discloses the apparatus of claim 1 wherein the trace information comprises a directed acyclic graph. [Figure 4, shows the dependency information included with the trace (sine the dependencies are based on the dependent operands such as in figure 2) that directly causes the scheduling shown in figure 7. This figure 4 shows that the information in each trace comprises a directed acyclic graph because the trace comprises instructions with a line between other instructions showing the dependency (sequential dependency) between them and not returning to the starting instruction, which meets the definition set forth in the specification on page 5, line 24 – page 6, line14.]

8. In regard to claim 3, Nair discloses the apparatus of claim 1 wherein the trace information includes pointers to the interdependent instructions. [Section 2.5 and the figures therein shows that the instructions are placed in slots for execution to be executed as soon as possible and that the program counter stays fixed on the first instruction in the sequence comprising the group or trace. Therefore, it is inherent that the instruction slots (which are included with the trace information as shown in figure 7) include pointers to the next slot to execute the instructions held there.]

9. In regard to claim 5, Nair discloses the apparatus of claim 1 wherein the interdependent instructions include the criterion instruction and instructions preceding the criterion instruction in the program sequence, as shown in figure 7.

10. In regard to claim 6, Nair discloses the apparatus of claim 1 wherein the interdependent instructions are classified into subslice types, the trace information including a pointer to each subslice that is formed by each type of the interdependent instructions. [Figure 7 shows how the instructions are divided and classified into different slots or subslice types. Section 2.5 and the figures therein shows that the instructions are placed in slots for execution to be executed as soon as possible and that the program counter stays fixed on the first instruction in the sequence comprising the group or trace. Therefore, it is inherent that the instruction slots (which are included with the trace information as shown in figure 7) include pointers to the next slot to execute the instructions held there.]

11. In regard to claim 7, Nair discloses the apparatus of claim 6 wherein each subslice is stored as dependent pieces. [Figure 7 shows that there are dependencies between instructions in different slots as described above.]

12. In regard to claim 8, Nair discloses the apparatus of claim 1 wherein the first triggering condition comprises a triggering instruction in the program sequence. [As shown above, the triggering condition is the occurrence of the speculated branch instruction.]

13. In regard to claim 9, Nair discloses the apparatus of claim 8 wherein the first triggering condition is based on evaluation of an architectural state. [As shown above,

the triggering condition is the branch instruction and thus the occurrence or decoding of this instruction in the architecture is the evaluated state therein.]

14. In regard to claim 10, Nair discloses the apparatus of claim 8 wherein the first triggering condition is based on evaluation of a micro-architectural state. [As shown above, the triggering condition is the branch instruction and thus the occurrence or decoding of this instruction in the micro-architecture is the evaluated state therein.]

15. In regard to claim 15, Nair discloses the apparatus of claim 1 wherein the plurality of traces includes a second trace and a third trace, wherein the second and third traces are independent of each other and adjacent in the program sequence, and further comprising grouping the second trace and the third trace into a very-long-instruction-word for parallel executions. [As shown above and in sections 1.1 and 2.1, the instructions in the traces of figure 7 are each renamed or reformatted instructions based on a past pre-execution. Thus each instruction in itself is a trace of the length of one instruction. Therefore within the trace of slot 0 in figure 7, there is for example two independent (no dependencies) subsequent second and third traces in the lwz instructions. It is shown that these instructions original program order were subsequent at numbers 4 and 5. Figure 7 shows that these traces have been combined into a single larger trace or LIW (long instruction word), which may also be called a very long instruction word.]

16. In regard to claim 16, Nair discloses the apparatus of claim 1 wherein traces of the plurality of traces that are data dependent of each other are chained together for serial executions. [Figure 7 shows that the trace in slot 3 is dependent on the trace in

slot 2 due to the reading of register 6.2 in slot 3 and the writing to it in slot 2. The figure also shows that the trace in slot 3 is chained serially after slot 2.]

17. In regard to claim 17, Nair discloses the apparatus of claim 1 further comprising an instruction pointer that indexes the trace information, the instruction pointer pointing to a first instruction or a last instruction of the interdependent instructions. [The second paragraph before section 2.5.1 on page 19 states that a program counter (instruction pointer) remains pointed to the first instruction in the sequence as it executes.]

18. In regard to claim 18, Nair discloses the apparatus of claim 1 further comprising: a main pipeline executing the program sequence; and at least one secondary pipeline disjoint from the main pipeline configured to speculatively execute the interdependent instructions associate with the first trace. [Figure 1 shows that there are two pipelines or engines, a primary (main) and a parallel (secondary). The primary engine determines the cacheable sequences of instructions to be scheduled by the translator, executes certain special instructions in the program sequence, and is used sparingly as a safety net. In addition, the first paragraph of page 14 shows that the primary engine initially executes the program sequence. The parallel engine implements the rest of the code, as shown in both these sections, which entails the trace execution of interdependent instructions. As shown previously and in section 2.6, branches are executed speculatively.]

19. In regard to claims 20-39, as indicated by Applicant, similar limitations exist as provided above for claims 1-3, 5-10, and 15-18 and thus the same arguments presented above apply.

20. Claim 20 is different from the previous claims in that it states limitations for identifying a pre-selected number of initial candidate instructions preceding the criterion instruction in the program sequence and determining which of the initial candidate instructions are associated instructions, wherein an outcome of the criterion instruction depends on the results of the associated instructions. Figure 7 of Nair shows that the lwz instruction (a criterion instruction as given above) of slot 2 is preceded in program sequence by other instructions, which have been identified and placed in the trace. The addic instruction of slot 1, for example, is an associated instruction where the outcome of the criterion instruction depends on the results of that instruction, which are stored in register 26.1.

21. Claim 29 is substantially the same in scope as claim 20 and the same arguments apply.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair in view of Killian (6,092,187).

24. In regard to claim 11,

a. Nair discloses the apparatus of claim 1.

b. Nair does not disclose wherein the one or more processors further determine a confidence metric of trace information associated with a specific trace, and wherein the confidence metric is indicative of a likelihood of producing a correct result from executing the specific trace.

c. Killian has shown in column 5, lines 32-36, that a trace cache uses confidence levels (metrics). These confidence levels predict the likelihood of producing a correct prediction as shown in column 3, lines 59-65. Killian shows in lines 64-65 that a larger confidence value yields greater confidence in a prediction.

d. It is well known in the art that greater confidence in a prediction is desirable. This greater confidence would have motivated one of ordinary skill in the art to modify the design of Nair to use the confidence levels taught by Killian. With this modification, the instructions or information in the traces are assessed with a confidence metric.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Nair to include the confidence level system taught by Killian so that greater confidence in the instruction predictions of traces can be realized.

25. In regard to claim 12, Nair in view of Killian discloses the apparatus of claim 11 wherein the confidence metric indicates whether or not the specific trace should be replaced by a new trace storing information about different instructions. [The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the

trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones.]

26. In regard to claim 13, Nair in view of Killian discloses the apparatus of claim 11 wherein the confidence metric indicates whether or not the specific trace should be rebuilt using new information about a criterion instruction associated with the specific trace. [The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones. Thus the trace that is sent for execution must be replaced or rebuilt. Since all traces use information from the criterion instruction to know where the trace ends. The trace is rebuilt using information from this criterion instruction.]

27. In regard to claim 14, Nair in view of Killian discloses the apparatus the apparatus of claim 11 further comprising a counter having a counter value that indicates the number of times the specific trace has been executed, the counter value, when exceeding a frequency threshold associated with the specific trace, triggering the specific trace to be rebuilt. [Column 15, lines 56-59 of Killian show the use of counters for prediction as taught in the background. Here in column 3, lines 59-67, it is shown that a suggested confidence level measure is using a counter to keep track of the number of executions of the trace without a misprediction. The threshold here is zero. When a misprediction is encountered the counter is reset to zero and the more correct

predictions the higher the confidence level. The confidence level system taught by Killian shows in column 5, lines 16-31, that if a prediction is not acceptable (low confidence) a second predictor replaces it. Since the trace cache is controlled by the confidence levels and predictions are made by the traces, if the predictor is changed, that means the trace and all its instructions are replaced with new ones. With the confidence level surpassing the threshold at zero, there is no confidence and a different predictor (trace) will be selected or rebuilt for execution.]

28. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nair in view of Tullsen et al (Simultaneous Multithreading: Maximizing On-Chip Parallelism).

29. In regard to claim 19,

a. Nair discloses the apparatus of claim 1 wherein the interdependent instructions associated with the first trace are executed by a secondary thread on a pipeline, and the program sequence is executed by a main thread on a pipeline. [Figure 1 shows that there are two pipelines or engines, a primary (main) and a parallel (secondary). The primary engine determines the cacheable sequences of instructions to be scheduled by the translator, executes certain special instructions in the program sequence, and is used sparingly as a safety net. In addition, the first paragraph of page 14 shows that the primary engine initially executes the program sequence. The parallel engine implements the rest of the code, as shown in both these sections, which entails the trace execution of interdependent instructions.]

b. Nair does not disclose that the two threads are on the same pipeline.

c. Tullsen has taught a simultaneous multithreading implementation, throughout the disclosure, which entails executing multiple threads in parallel on a single pipeline.

d. The first paragraph of section 6 shows that the SM (simultaneous multithreading) processor requires fewer resources relative to multiprocessing, in order to achieve the same desired level of performance. The ability to use fewer resources while not sacrificing performance would have motivated one of ordinary skill in the art at the time of invention to modify the design of Nair to use simultaneous multithreading as taught by Tullsen.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Nair to use the simultaneous multithreading technique taught by Tullsen for the two processing engines so that fewer system resources are used while not sacrificing performance.

Response to Arguments

30. Applicant's arguments filed 9/27/04 have been fully considered but they are not persuasive.

31. Applicant has argued on pages 20-21 that Nair does not disclose each of the plurality of traces including information indicative of interdependent instructions. The traces of Nair shown in figure 7 include the interdependent instructions, which is information indicative or identifying the interdependent instructions.

32. Applicant then points to figure 7 of Nair as showing that all the groups do not include criterion instructions as recited in claim 1. Claim 1, however, does not disclose

that all the groups or traces of figure 7 must include a criterion instruction. The claim only states that each of the plurality of traces (where the plurality of traces can and will be interpreted as each group or trace of figure 7 that includes a criterion instruction) includes information indicative of interdependent instructions, where this information is the interdependent instructions themselves as shown above. The specification defines a criterion instruction in the replacement paragraph (for the paragraph beginning on page 4, line 18) on page 3 of the previous amendment of 4/12/04 to be a branch or a load that can incur long latency when executed. Traces or groups 0-3 are a plurality of traces and each contain a criterion instruction according to this definition.

33. The arguments for claim 20 also state that Nair illustrates that groups or traces need not include criterion instructions. This is overcome for the same reason as given above for claim 1. This then overcomes the problem of those groups not identifying a pre-selected number of initial candidate instructions preceding the criterion instruction in the program sequence. Figure 7 of Nair shows that the lwz instruction (a criterion instruction as given above) of slot 2 is preceded in program sequence by other instructions, which have been identified and placed in the trace. The addic instruction of slot 1, for example, is an associated instruction where the outcome of the criterion instruction depends on the results of that instruction, which are stored in register 26.1.

Conclusion

34. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited in the previous action remain pertinent and are cited herein as well.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
October 26, 2004

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